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Electrical properties of ultrathin HfO_2 gate dielectrics on partially strain compensated SiGeC/Si heterostructures

R. Mahapatra · S. Maikap · S. K. Ray

Abstract Ultrathin HfO_2 gate dielectrics have been deposited on strained $Si_{0.69}Ge_{0.3}C_{0.01}$ layers by rf magnetron sputtering. The polycrystalline HfO_2 film with a physical thickness of ∼6.5 nm and an amorphous interfacial layer with a physical thickness of ∼2.5 nm have been observed by high resolution transmission electron microscopy (HRTEM). The electrical properties have been studied using metal-oxide-semiconductor (MOS) structures. The fabricated MOS capacitors on $Si_{0.69}$ $Ge_{0.3}C_{0.01}$ show an equivalent oxide thickness (EOT) of 2.9 nm, with a low leakage current density of $\sim 4.5 \times 10^{-7}$ A/cm^2 at a gate voltage of –1.0 V. The fixed oxide charge and interface state densities are calculated to be 1.9×10^{12} cm^{-2} and 3.3×10^{11} cm^{-2}eV^{-1}, respectively. The temperature dependent gate leakage characteristics has been studied to establish the current transport mechanism in high-k HfO_2 gate dielectric to be Poole–Frenkel one. An improvement in electrical properties of HfO_2 gate dielectrics has been observed after post deposition annealing in O_2 and N_2 environments.

Keywords High-k · HfO_2 · Gate dielectric · SiGeC

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1 Introduction

The rapid progress of complementary metal-oxide-semiconductor (CMOS) technology has driven the down-scaling of device dimension to nano-regime [1]. One of the more fundamental limits is the scaling of the gate oxides due to the exponential increase in tunneling current with decreasing oxide thickness. These limitations have led to an increased interest for the deposited high dielectric constant (high-κ) gate materials with low leakage current, good thermal stability and interface characteristics comparable to SiO_2/Si interface. Intensive studies on alternative gate dielectrics with high permittivity, such as HfO_2 [2–4], ZrO_2 [5, 6], Al_2O_3 [7], their silicates [8, 9] and nitrides [10, 11] are being made to overcome the excessive leakage current and reliability issues of conventional SiO_2 gate dielectrics in MOS devices. Considerable attention has been given to HfO_2 due to its relatively high dielectric constant (16–45), wide band gap (∼5.8 eV) and its compatibility with $n^{\pm}$ polysilicon gate electrode material [12–14]. Furthermore, as the Gibbs energy of formation of HfO_2 is more negative than ZrO_2 (−1088 kJ/mol vs −1040 kJ/mole) [15], it appears to be thermally stable at temperatures of up to 1000°C.

In recent years, partially strain compensated SiGeC alloy layers are being utilized in Si-based band gap engineered heterostructure devices [16–18]. These alloy layers are promising candidates for low-power and high-speed semiconductor devices, because of their higher hole mobility [19, 20]. However, the study of formation of an oxide layer on SiGeC alloys using conventional thermal oxidation showed the preferential oxidation of Si, leading to the formation of Ge-rich layers and C precipitation at the oxide/substrate interface [21]. This Ge-rich layer causes high fixed oxide charge and interface state density, and poor breakdown characteristics of SiGeC based MOSFETs. HfO_2 is attractive as a high-k gate

dielectric on SiGeC alloys by alleviating the above problems because of low thermal budget processing reported in literature [14, 22, 23].

In this study, we report the electrical characteristics in terms of dielectric constant, equivalent oxide thickness (EOT), and current transport mechanisms to examine the potential of HfO_2 as an alternative gate dielectric for SiGeC MOSFET applications. The effect of post-deposition annealing is reported to study the thermal stability of HfO_2 gate dielectrics on silicon heterolayers.

2 Experimental

Epitaxial $Si_{0.69}Ge_{0.3}C_{0.01}$(∼40 nm thick) films, grown by ultra-high vacuum chemical vapor deposition (UHVCVD) on Si-buffer layer (∼50 nm) at 550°C at a base pressure of 1×10^{-10} Torr using SiH_4, GeH_4 and CH_3SiH_3 were used in this study.High-resolution X-ray diffraction and Raman spectra have shown the growth of strain-compensated epitaxial layers with C incorporated in substitutional sites. The samples were subjected to a standard cleaning schedule followed by a dip in dilute HF for 1 min to remove the native oxide and to terminate the surface with hydrogen prior to the dielectric film deposition. The film was deposited on $Si_{0.69}Ge_{0.3}C_{0.01}$/Si heterolayers by rf magnetron sputtering from a 2 inch. diameter HfO_2 target at a power of 50 W with a base pressure of 5×10^{-6} Torr. Reactive sputtering was performed at a substrate temperature of 350°C in an Ar (∼16 sccm) and O_2 (∼7 sccm) ambient keeping the operating pressure at 15 mTorr. HfO_2 films on partially strain compensated $Si_{0.69}Ge_{0.3}C_{0.01}$ layer were annealed in both nitrogen and oxygen ambient at temperatures in the range of 500°C–800°C for 15 min to study their thermal stability.

Electrical properties of HfO_2 films were studied using fabricated Al-gate (area: 1.26×10^{-3} cm^2) metal-oxide-semiconductor (MOS) structures with programmable Keithley-590 C-V analyzer, Keithley-485 pico-ammeter and Advantest-R6144 constant dc voltage source. The post-metal annealing was done in N_2 ambient at 400°C for 15 min to reduce the contact resistance.

3 Results and discussion

The interfacial structure and thickness of HfO_2 films were obtained by high resolution transmission electron microscopy (HRTEM) using a JEM 3000F field emission system with an operating voltage of 300 kV and a resolution of 0.17 nm. Figure 1 shows the typical cross-sectional TEM image of an as-deposited HfO_2 film on SiGeC/Si heterostructure. The micrograph exhibits an upper layer (UL) polycrystalline HfO_2 film with a physical thickness of ∼6.5 nm and an amorphous interfacial layer (IL) with a thickness of ∼2.5 nm. The

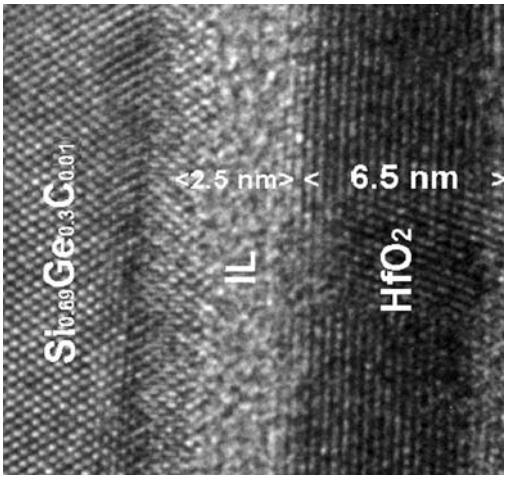

Fig. 1 Typical cross-sectional TEM image of HfO_2 film deposited on $Si_{0.69}Ge_{0.3}C_{0.01}$ layer at a substrate temperature 350°C

relatively thick interfacial layer is likely to be formed because HfO_2 was sputtered from a Hf-oxide target in an Ar/O_2 gas mixture.

Figure 2 shows the high frequency (100 kHz) C-V characteristics of fabricated MOS capacitors using HfO_2 with thickness of ∼9.0 nm. A well-behaved C-V characteristics is obtained with a relatively low value (−1.0V) of flat-band voltage (V_{fb}), indicating the absence of any Ge pileup or Ge segregation [24] at HfO_2/SiGeC interface. From the accumulation capacitance, the equivalent oxide thickness (EOT) is found to 2.9 nm. . The fixed oxide charge and interface state densities are calculated to be 1.9×10^{12} cm^{-2} and 3.3×10^{11} cm^{-2} eV^{-1}, respectively, which are comparable to reported results [25, 26]. The leakage current characteristic of MOS

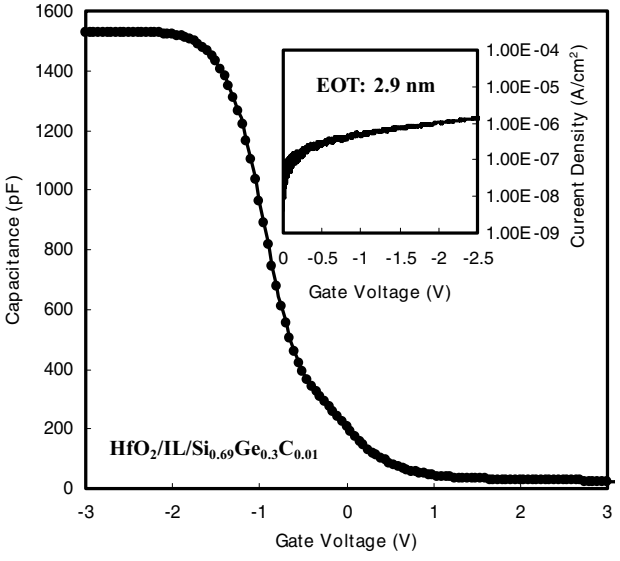

Fig. 2 High frequency (100 kHz) C-V characteristics of fabricated MOS capacitors using HfO_2 films on $Si_{0.69}Ge_{0.3}C_{0.01}$ heterolayers. Leakage current characteristic of HfO_2 with interfacial layer is shown in the inset

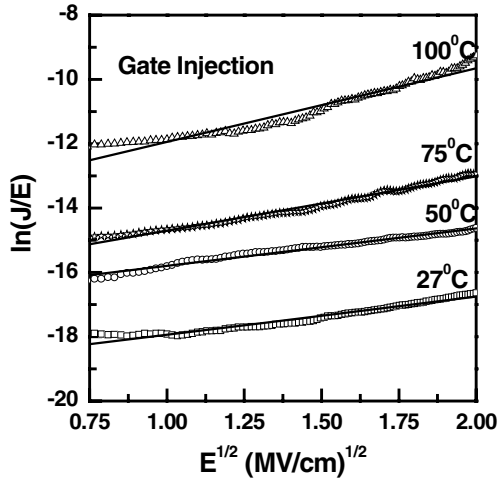

Fig. 3 The PF plot of J-V curve for different temperatures under gate electron injection (negative V_g)

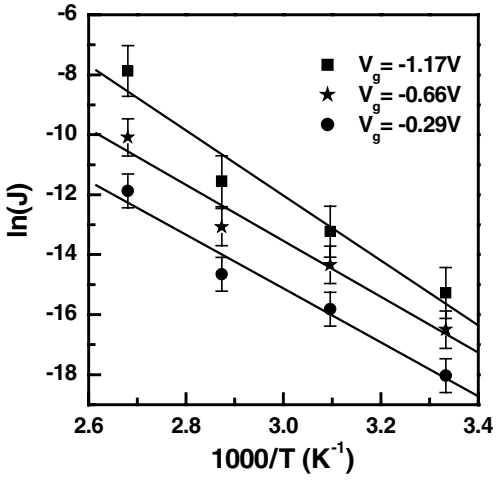

Fig. 4 Arrhenius plot (lnJ vs 1000/T) under different gate voltages of $Al/HfO_2/Si_{0.69}Ge_{0.3}C_{0.01}/Si$ MOS capacitors

capacitors using HfO_2 gate dielectric on $Si_{0.69}Ge_{0.3}C_{0.01}$ layer with an EOT of 2.9 nm is shown in the inset of Fig. 2. The measured current density is about $\sim 4.5 \times 10^{-7}$ A/cm^2 at –1 V gate bias. The value of the leakage current is several orders lower, as compared to SiO_2 of the same EOT [27], which keeps the devices away from the fundamental limit faced using conventional gate oxides.

The temperature dependent gate leakage characteristics were studied to understand the current transport mechanisms in HfO_2 on strained SiGeC/Si heterolayer. Figure 3 shows the Poole-Frenkel (PF) plot of the current density-voltage (J-V) curve for different temperatures under an electron injection from the gate (negative V_g). The PF conduction model is fitted well though there is a little deviation for operating temperature on or above 100°C. The current is given by

$$J = CE \exp\left[\frac{-q(\Phi - \beta_{PF}\sqrt{E})}{\xi kT}\right]$$

where C and k are the proportionality and Boltzmann constant, respectively. $q\phi$ is the ionization potential in eV, which is the amount of energy required for the trap electron to escape the influence of the positive nucleus of the trapping center without any applied field. $\beta_{PF}\sqrt{E}$ is the amount by which the trap barrier height is reduced by the applied electric field, E. The factor ξ in the denominator of the exponential may vary between 1 and 2, depending on the amount of acceptor concentration [28]. In order to have further insight into the conduction mechanism, the Arrhenius plot (lnJ vs 1000/T) under different gate voltages has been shown in Fig. 4. The logarithmic current is inversely proportional to the temperature with some deviation at high temperature. Thus the dominant current conduction mechanism through the HfO_2 films

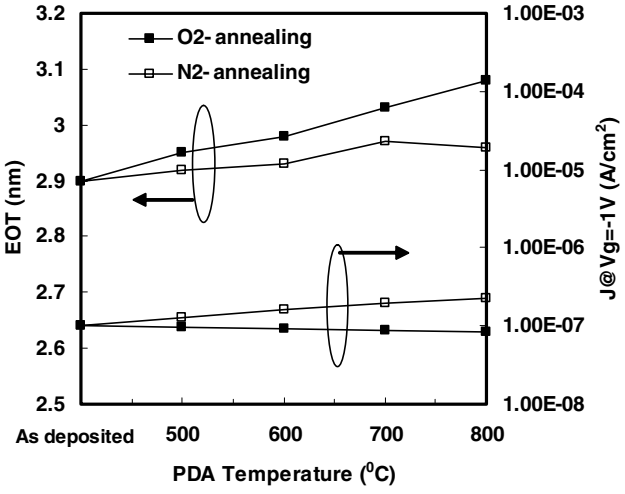

Fig. 5 Variation of EOT and current density (@ $V_g = -1$V) of $Al/HfO_2/Si_{0.69}Ge_{0.3}C_{0.01}/Si$ MOS capacitors as a function of post-deposition annealing temperatures for HfO_2 gate dielectrics

on SiGeC heterolayer is of PF type, in agreement with the reported result [29].

Figure 5 shows the variation of EOT extracted from the accumulation capacitance and leakage current density (@ $V_g = -1$V) with post deposition annealing (PDA) temperatures. As seen from Fig. 5, the change of EOT is much less for N_2 annealing though the leakage current density is found to be lower in O_2 annealed samples. This is due to the increase of interfacial layer thickness during O_2 annealing [30, 31] which, consequently, leads to the reduction of the leakage current density.

Figure 6 shows the hysteresis width in C-V characteristics and interface trap densities at the $HfO_2/Si_{0.69}Ge_{0.3}C_{0.01}$ interface as a function of annealing temperature in O_2 and N_2 ambients. The counterclockwise C-V curve is produced by charge trapping under negative gate bias. Hysteresis width

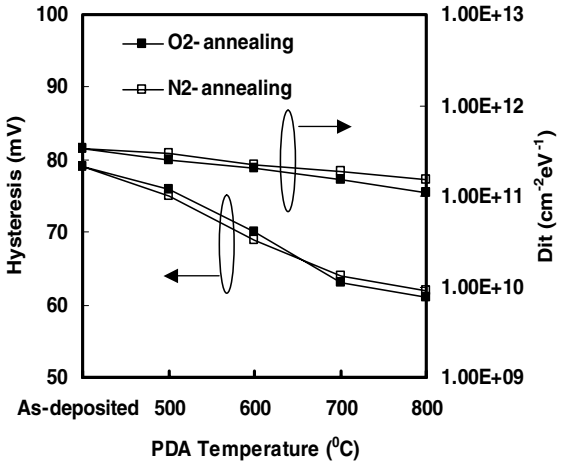

Fig. 6 Hysteresis width and interface trap densities of the $HfO_2/Si_{0.69}Ge_{0.3}C_{0.01}$ interface as a function of annealing temperature

(V_{hy}) of the as-deposited gate dielectric is 79 mV, which decreases with increasing PDA temperature in O_2 and N_2 ambient. Relatively small V_{hy} values (∼60 mV) suggest that the post deposition annealing leads to the reduction of trapped charge density. As observed through hysteresis study, the interface trap densities of HfO_2 thin films decrease with increasing PDA temperature.

4 Conclusions

Ultrathin HfO_2 gate dielectrics have been deposited on strained $Si_{0.69}Ge_{0.3}C_{0.01}$ layers by rf magnetron sputtering. The formation of an interfacial layer has been observed by high resolution transmission electron microscopy. The leakage current density of HfO_2 gate dielectrics is found to be several orders of magnitude lower than that reported for thermal SiO_2 with the same equivalent thickness. The temperature dependence of the gate leakage current has been studied to understand the current transport mechanisms in high-k HfO_2 gate dielectric films on strained SiGeC layer. The logarithmic current is found to be inversely proportional to the temperature that agrees with the Poole–Frenkel model. A better thermal stability of electrical properties of HfO_2 gate dielectrics has been observed after post deposition annealing. However, the annealing in O_2 would cause the increase of EOT more significantly.

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